R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the claims as originally filed, for example, claim 9 and in the specification as originally filed, for example, on page 6, line 15 through page 7, line 2 and on page 7, line 19 through page 8, line 9. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-4, 6-8, 10, 11, 15-17 and 20-23 under 35 U.S.C. §102 as being anticipated by Lien et al. (U.S. Patent No. 6,211,697, hereafter Lien) is respectfully traversed and should be withdrawn.

Lien is directed to an integrated circuit that includes a field programmable gate array and a hard gate array having the same underlying structure (Title of Lien).

In contrast, the presently claimed invention (claim 1) provides one or more logic circuits comprising (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device.

Claims 15 and 16 include similar limitations. Lien does not disclose or suggest non-programmable hard wired blocks, as presently claimed. Therefore, Lien does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, assuming *arguendo*, the elements 210-216 in FIG. 9b of Lien are similar to the presently claimed non-programmable hard wired blocks (as suggested on page 2, section 2, lines 6-7 of the Office Action and for which Applicant's representative does not necessarily agree), Lien does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. In particular, Lien describes the elements 210-216 as hard gate arrays (HA) (column 4, lines 36-47 and column 11, lines 30-35 of Lien). Lien further provides that a hard array is a mask metal **programmable** gate array which is **programmed** during the IC chip manufacturing process (column 4, lines 42-44 of Lien). Lien clearly discloses that the field **programmable** gate array and the mask metal **programmable** hard arrays have the same underlying structure (Title, abstract, and column 4, lines 53-54 of Lien). The ICs 20, 200 and 208 of Lien include both field **programmable** gate arrays that are **programmed** by

configuration data stored in memory and mask metal **programmable**, or "hard", gate array that are **programmed** by configuration data stored as hard-wired connections (column 4, line 65 through column 5, line 2 of Lien).

In contrast to the position taken in the Office Action, one skilled in the art would understand the mask metal programmable gate arrays (i.e., elements 20, 202, 204 and 210-216) of Lien to be **programmable**. (See paragraphs 8-12 of the Declaration of Michael T. Moore pursuant to 37 CFR §1.132 attached hereto and column 4, lines 40-45 of Lien). Furthermore, one skilled in the art would not consider the non-programmable hard wired blocks, as presently claimed, to refer to programmable (either field-programmable or mask metal programable) gate array logic as contained in Lien (see paragraphs 8 and 13 of the Declaration of Michael T. Moore pursuant to 37 CFR §1.132 attached hereto). Therefore, Lien does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over Lien and the rejection should be withdrawn.

With respect to claim 2, the conclusory statement that all circuits have variable width fails to adequately address or make specific findings to factually support the conclusion that Lien inherently shows one or more logic circuits comprising

variable width logic circuits as presently claimed. Specifically, the Office Action fails to present any factual evidence or convincing line of reasoning why one skilled in the art of the present invention would understand Lien as necessarily including variable width logic circuits, as presently claimed. Therefore, the Office Action fails to factually establish a *prima facie* case of anticipation. As such, the presently pending claim 2 is fully patentable over the cited reference and the rejection should be withdrawn.

With respect to claim 3, the Office Action fails to present any factual evidence or convincing line of reasoning why the signals INPUT 1 - INPUT D in FIG. 5 of Lien are considered to be determinative of the width of each of the one or more logic circuits (see the last two lines on page 2 of the Office Action). Therefore, the Office Action fails to factually establish a *prima facie* case of anticipation. As such, the presently pending claim 3 is fully patentable over the cited reference and the rejection should be withdrawn.

With respect to claim 6, the Office Action fails to present factual evidence or a convincing line of reasoning why one skilled in the art would understand the reference to the Joint Test Action Group (JTAG) in column 12, lines 50-67 of Lien, as necessarily referring to performing a cyclic redundancy check

function, as presently claimed (see page 3, lines 4-6 of the Office Action). Therefore, the Office Action fails to factually establish a *prima facie* case of anticipation. As such, the presently pending claim 6 is fully patentable over the cited reference and the rejection should be withdrawn.

With respect to claim 11, the conclusory statement that Lien shows a number of registers configured to increase a throughput of one or more logic circuits (see page 3, lines 14-15 of the Office Action) fails to present any evidence or convincing line of reasoning why one skilled in the art would consider the D flip-flops in FIG. 13 of Lien to be configured to increase a throughput of one or more logic circuits, as presently claimed (see page 3, lines 14-15 of the Office Action). Therefore, the Office Action fails to factually establish a *prima facie* case of anticipation. As such, the presently pending claim 11 is fully patentable over the cited reference and the rejection should be withdrawn.

With respect to claims 21 and 22, the statement in the Office Action on page 3, lines 17-18 that the apparatus described above is applicable to the method claims 20-22 does not adequately address the specific limitations of claims 21 and 22. In particular, claims 21 and 22 are directed to an apparatus, not a method. The Office Action fails to specifically address how the

cited reference is applied to the specific limitations of claims 21 and 22. Therefore, the Office Action fails to factually establish a *prima facie* case of anticipation. As such, the presently pending claims 21 and 22 are fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, with respect to claim 21, the presently pending claim 21 recites, "wherein said non-programmable hard wired blocks comprise dedicated logic having a fixed implementation of a given functional block on silicon." The Office Action fails to address why the language "dedicated logic" is read on by Lien in light of the Declaration of Michael T. Moore pursuant to 37 CFR §1.132 filed with paper no. 10 on July 18, 2003. Specifically, paragraph 14 of the Declaration of Michael T. Moore filed on July 18, 2003 and paragraph 13 of the Declaration of Michael T. Moore under 37 CFR §1.132 attached hereto, state that the term "dedicated logic", "hard wired block" and "non-programmable logic element" would not be understood in the art to refer to a programmable (either field programmable or mask metal programmable) gate array logic. Since Lien is directed to a field-programmable gate array and a mask metal programmable gate array having the same underlying structure, it follows that Lien does not disclose dedicated logic having a fixed implementation of a given functional block on silicon, as presently claimed. As such, the presently pending

claim 21 is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, MPEP §707.07(d) states:

> "Where a claim is refused for any reason relating to the merits thereof it should be 'rejected' and the ground of the rejection **fully and clearly stated** . . . ." (MPEP §707.07(d), emphasis added).

In particular, the statement on page 3, lines 17-18 of the Office Action does not fully and clearly state the ground of the rejection. Specifically, the Office Action does not apply the Lien reference to the specifically claimed limitations of the rejected claims. Therefore, the Office Action does not appear to meet the Office's own requirements for properly rejecting claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, since the Office Action does not fully and clearly explain how the Lien reference applies to the specifically claimed limitations of each of the previously presented claims 20-22 (see page 3, lines 17-18 of the Office Action), a final rejection in the next Office Action would not be proper. Specifically, MPEP §706.07 states:

> **Before final rejection is in order** a clear issue should be developed between the examiner and the applicant. To bring the prosecution to as speedy conclusion as possible and at the same time to deal justly by both the applicant

> and the public, the invention as disclosed and claimed should be thoroughly searched in the first action and **the references fully applied**; . . . . MPEP §706.07 (emphasis added).

Because the Office Action does not fully and clearly explain how the Lien reference is applied to the specifically claimed limitations of all the previously presented claims, the Office Action neither (i) develops a clear issue between the Examiner and the Applicant nor (ii) fully applies the cited reference. Therefore, the next Office Action should be non-final.

Claims 2-14 and 17-24 depend, either directly or indirectly, from claim 1 or claim 16 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 5, 9, 12, 13, 18, 19 and 24 under 35 U.S.C. §103 as being unpatentable over Lien in view of Kaptanoglu (U.S. Patent No. 5,448,185) is respectfully traversed and should be withdrawn.

Claims 5, 9, 12, 13, 18, 19 and 24 depend, either directly or indirectly, from claims 1 or 16 which are believed to allowable. As such, the presently claimed invention is fully

patentable over the cited references and the rejection should be withdrawn.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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(586) 498-0670

Dated: May 7, 2004

Docket No.: 0325.00361

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael T. Moore		
Assignee:	Cypress Semiconductor Corporation		
Title:	CONFIGURABLE DEDICATED LOGIC IN CPLDs		
Serial No.:	09/804,523	Filed:	March 12, 2001
Examiner:	Tran, A.	Art Unit:	2819
Attorney Docket No.:	0325.00361		

Comissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF MICHAEL T. MOORE PURSUANT TO 37 C.F.R. § 1.132

I, Michael T. Moore hereby declare as follows:

1. I am presently employed as a Patent Agent by Cypress Semiconductor Corporation.

2 I have been employed by Cypress since August 1998 in various capacities including an Application Engineer and a Senior Application Engineer.

3. I have reviewed both (i) the claims of the present invention and (ii) U.S. Patent No. 6,211,697 to Lien et al.

4. I understand that in one embodiment the present invention concerns:

An apparatus comprising:

one or more logic circuits configured to provide logical operation, wherein said one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

5. I understand that in another embodiment the present invention concerns:

An apparatus comprising:

means for receiving one or more input signals; and

means for performing logical operation on said input signals using (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

6. I understand that in another embodiment the present invention concerns:

A method for computing in a programmable logic device (PLD) comprising the steps of:

(A) receiving one or more input signals;

(B) performing logical operation on said one or more input signals with (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable elements within said programmable logic device, wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

7. U.S. Patent No. 6,211,697 to Lien et al. does not disclose and would not suggest a non-programmable hard wired block having no programmable elements, as presently claimed.

8. Based upon my experience and work in the field of semiconductors, a mask metal programmable gate array as contained in Lien et al. would not be considered a non-programmable block or logic element.

9. Specifically, a hard gate array (HA) as disclosed in Lien is known in the art as a type of mask-programmable logic array (See "98. Array Circuit Types", Electronics Engineers' Handbook, Third Ed., McGraw-Hill, Inc., 1989, page 8-102-103; attached as Exhibit A).

10. A hard gate array as disclosed in Lien et al. contains a number of uncommitted gates which can be interconnected (i.e., programmed) by application of one or more metal layers to form a custom-circuit logic function (See the definition of Gate Array on page 8-103 in Exhibit A, column 4, lines 42-47 and column 4, line 65 through column 5, line 2 of Lien et al.).

11. Even after a gate array has been programmed, a number of the gates (i.e., programmable elements) can remain uncommitted (i.e., programmable).

12. A hard gate array can be reprogrammed by adding additional mask layers or etching the previously formed metal layers.

13. The terms dedicated logic, hard wired block, and non-programmable logic element would not be understood in the art to refer to a programmable, either field-programmable or mask metal programmable, gate array logic.

14. I hereby declare that all statements made herein of my knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or patents issued therefrom.

Michael T Moore Date: 5/7/04

Michael T. Moore

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Exhibit A

Electronics Engineers' Handbook

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Third Edition

McGRAW-HILL BOOK COMPANY

New York St. Louis San Francisco Auckland Bogotá
Hamburg London Madrid Mexico
Milan Montreal New Delhi Panama
Paris São Paulo Singapore
Sydney Tokyo Toronto

Library of Congress Cataloging-in-Publication Data

Electronics engineers' handbook.

Includes index.
1. Electronics—Handbooks, manuals, etc. I. Fink, Donald G. II. Christiansen, Donald.
TK7825.E34 1989 621.381'0202 88-13187
ISBN 0-07-020982-0

34567890 DOC/DOC 93210

ISBN 0-07-020982-0

The editors for this book were Daniel A. Gonneau and Lucy Mullins, the designer was Naomi Auerbach, and the production supervisor was Richard A. Ausburn. It was set in Times New Roman by University Graphics, Inc.

Printed and bound by R. R. Donnelley & Sons Company.

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trajectory through the silicon the α particle generates roughly 1.2 million electron-hole pairs. Some percentage of the electrons generated will find their way to the surface and be collected by memory-cell nodes. If the number collected by any one node is large, the voltage on the node may be reduced sufficiently to cause a misread or soft failure. One source of the α particles is the IC packaging material, and efforts are being made to reduce the α radiation to a minimum. Another possible solution is to coat the surface of the IC with a material that will stop the α particle from getting to the silicon surface.

Figure 8-159 shows the organization diagram for a dynamic MOS RAM. Reading and writing occur for all cells in one row simultaneously. Since only 1 bit at a time is available for writing, an internal read operation is used to transfer the data to the refresh amplifier before writing. In this manner, the refresh amplifier contains data corresponding to the contents of the row into which writing takes place.[101]

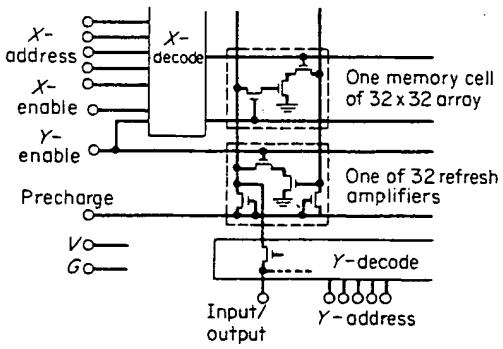

Fig. 8-159. Organization diagram of a dynamic MOS random-access memory system.

97. Shift Registers. A shift register is an arrangement of an arbitrary number of storage cells in a row and is used primarily for temporary storage of digital information. Some common applications of shift registers are in serial-data entry and serial-data output, as well as in serial-to-parallel converters. The serial-in–serial-out shift register can perform similarly to a high-speed drum memory; however, unlike the mechanical drum memory, it can be stopped instantaneously. Serial-to-parallel converters are often used in accumulators, where the data are entered in serial fashion, e.g., from a keyboard, and then acted upon in parallel, as by an adder.

The shift registers can be designed for either static or dynamic operation. Static shift registers make use of the basic flip-flop circuits of Figs. 8-146 and 8-147 for data-storage purposes. Dynamic shift registers operate in the same manner as the dynamic RAM circuits, where each bit of information is constantly refreshed and recycled. Figure 8-160 shows the circuit diagram of a section of a dynamic MOS shift-register circuit. The circuit operates with two-phase clock pulses, $V_{\phi 1}$ and $V_{\phi 2}$. After each clock pulse, one bit of information is inverted and transferred half a cell to the right; thus, after two clock pulses, the contents of each cell are shifted over to the next one.

98. Array Circuit Types. LSI logic arrays fall into two basic categories, *field-programmable* and *mask-programmable*,[109,110] each with important advantages and disadvantages. All field-programmable types have a fixed number of OR gates, AND gates, and sometimes flip-flops per circuit. Programming is handled through *fusible links* similar to those of a PROM. Advantages are that several custom logic functions can be developed from one IC part number by blowing the fuse links. Changes are easily incorporated by programming a new fuse pattern. Programming commonly requires special equipment, although some of the smaller array circuits use standard PROM programming hardware. Disadvantages of the fusible-link approach relate to the fixed pattern of inputs, outputs, and logic functions on chips. For example, an LSI circuit incorporating a 10-bit shift register cannot be built if the field-programmable circuit is limited to eight flip-flops. Similarly an LSI part requiring multiphase clocking cannot be built on an array which connects all flip-flops to a common clock line.

Mask-programmable arrays, commonly known as *gate arrays,* and *macrocell arrays* and sometimes called *master slices,* offer greater logic flexibility. Gate arrays have a large number of gates on chips which can be connected to build any logic function, subject only to package pins and

the number of gates. By interconnect elements can be placed in any combi

The *macrocell array* carries the cc complexity blocks, called macrocells library of macrocell functions and ne

Disadvantages of mask-programm option requires a custom metal patte having only custom metal is much s full semiconductor mask set, it is r location.

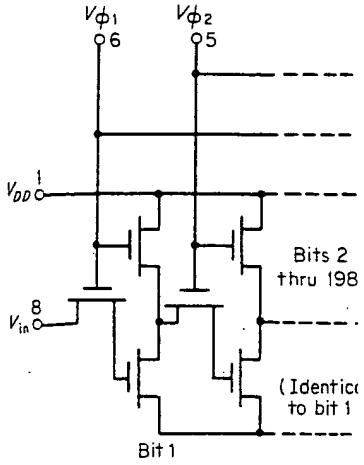

Fig. 8-160. Circuit diagr

Arrays approaching 1,200 gates ha generally better than with the mask with ECL arrays, is superior to other

The main purpose of logic arrays i LSI circuit. One way of comparing t circuit board and see how each repla

The *fusible-link arrays* equate to a sometimes flip-flops. The board is ful the gates implement various logic eq

The *gate array* is the same circuit gate packages. The designer than add function.

The analogy can be extended to m IC sockets and a data book full of lo data book (macrocell library), puts t routing channels.

A typical macrocell array has 85 l positions on the chips.

Array Terminology. The follow

Gate array: An IC containing a nu dedicated metal patterns to form a c and 1,200 gates and may use CMOS,

Macrocell: An array subsection p Macrocells normally relate to MSI cc adders, etc., and make design easier array or the basic building block in a

the number of gates. By interconnecting gates as flip-flops, adders, multiplexers, etc., these circuit elements can be placed in any combination anywhere on a chip.

The *macrocell array* carries the concept one step further by subdividing the array into MSI-complexity blocks, called macrocells, rather than individual gates. The designer works with a library of macrocell functions and need not implement everything from simple gates.

Disadvantages of mask-programmable arrays center around mask programming. Every circuit option requires a custom metal pattern on top of a standard semiconductor diffusion set. While having only custom metal is much simpler than a custom circuit designed from scratch with a full semiconductor mask set, it is more complex than programming with fuses at the user's location.

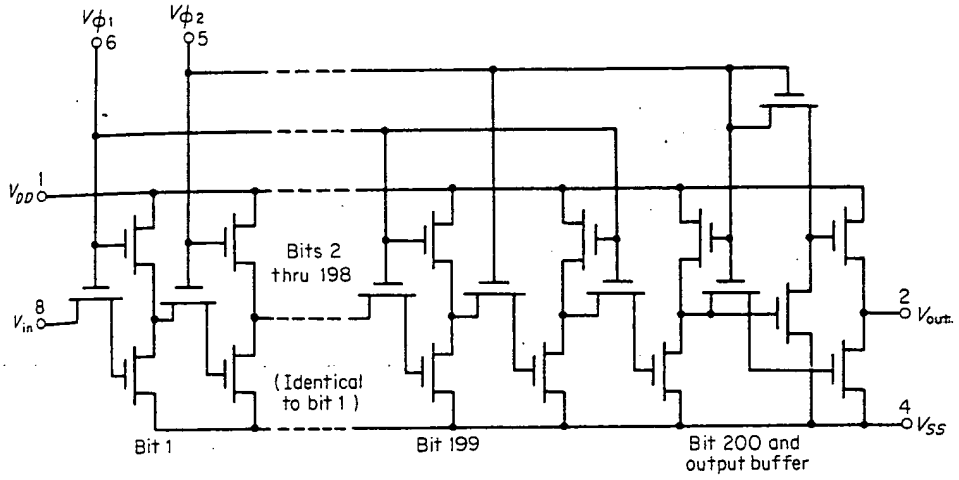

Fig. 8-160. Circuit diagram of one section of a 200-bit dynamic shift register.

Arrays approaching 1,200 gates have more logic power per package, speed-power products are generally better than with the mask programmable circuits, and circuit performance, especially with ECL arrays, is superior to other forms of digital logic.

The main purpose of logic arrays is to replace several IC packages on a circuit board with one LSI circuit. One way of comparing the array types is to visualize them as a miniature printed-circuit board and see how each replaces logic.

The *fusible-link arrays* equate to a circuit board with a combination of OR gates, AND gates, and sometimes flip-flops. The board is fully wired. The designer then cuts metal (fusible links) so that the gates implement various logic equations.

The *gate array* is the same circuit board populated with a large number of two- or three-input gate packages. The designer than adds metal, interconnecting the gates to implement the desired function.

The analogy can be extended to macrocell arrays by visualizing a circuit board full of empty IC sockets and a data book full of logic functions. The designer selects logic functions from the data book (macrocell library), puts them in the IC sockets, and interconnects the ICs through routing channels.

A typical macrocell array has 85 logic functions in a macrocell library and a total of 106 cell positions on the chips.

Array Terminology. The following definitions will be helpful:

Gate array: An IC containing a number of uncommitted gates which are interconnected with dedicated metal patterns to form a custom-circuit logic function. Gate arrays vary between 100 and 1,200 gates and may use CMOS, I^2L, TTL, or ECL circuit technologies.

Macrocell: An array subsection performing a higher-level logic function than a basic gate. Macrocells normally relate to MSI complexity circuits such as flip-flops, decoders, multiplexers, adders, etc., and make design easier than using gates. Macrocells can be several gates in a gate array or the basic building block in a more advanced macrocell array.